# Fast & Energy Efficient Binary to BCD Converter with Complement Based Logic Design (CBLD) for BCD Multipliers

# Abstract:

In this work, Complement Based Logic Design is introduced as a new logic design and optimization method for combinational circuits at the gate level. The classification of arithmetic building blocks for optimization with CBLD technique is investigated. The efficiency of this technique is demonstrated by applying CBLD on some of the arithmetic building blocks which have a potential of the optimization. Then a fast and energy-efficient Binary to BCD converter is designed by CBLD. This converter is a crucial building block for performing the decimal digit by digit multiplication in the binary system. In the proposed logic design of combinational circuits with multi-input-multi-output, each output is assigned by a selected input with two conditions, buffer or complement, controlled by a control function. Finding best input and output sets with the optimum control function as the condition of complement and repetition of this method to cover all the outputs can complete CBL design. The simulation results for proposed binary to BCD converter show an average Speed, Power Delay Product (PDP), Energy Delay Product (EDP) & Area-PDP (APDP) improvement of 53-67%, 29-66%, 38-86%, and 16-71%, respectively, for the proposed architecture compared with the referenced architectures in various selected technologies.

**Tools used:**

**Xilinx 13.2**